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EXAMINER	
LEE, RICHARD J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/942,607	Applicant(s) UETANI, YOSHIHARU	
	Examiner Richard Lee	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-19* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 3, 10, and 12-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For examples:

(1) claim 3, line 2, "device" should be changed to "processor" in order to provide proper antecedent basis for the same as specified at claim 1, line 11;

(2) claim 12, line 25, line 28, line 31, "decoding processors" should be changed to "decompression devices" in order to provide proper antecedent basis for the same as specified at line 4, respectively; and

(3) claim 14, line 2, "device" should be changed to "processor" in order to provide proper antecedent basis for the same as specified at claim 12, line 14.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (5,889,560) in view of Chida (6,313,863).

Lee discloses an MPEG video decoder as shown in Figure 1, and substantially the same decoding apparatus as claimed in claims 1 and 2, configured to decode compression-encoded video data in units of at least one block (see column 3), the video data including a variable length code comprising a variable length decoder (112 of Figure 1) which decodes the variable length code to output a zero-run length and a nonzero coefficient; an inverse quantizer (116 of Figure 1)

which inverse-quantizes the nonzero coefficient to output an inverse-quantized result; a zero-run reconstruction processor (118 of Figure 1) which reconstruct zero coefficients, the zero coefficients corresponding to the zero-run length; an inverse discrete cosine transformer (130 of Figure 1) which subjects the reconstructed coefficients and inverse quantized coefficient to an inverse discrete cosine transformation to output a transformed result; and a motion compensator (150 of Figure 1) which subjects the transformed result to a motion compensation; wherein the variable length decoder decodes the variable length code corresponding to a macro block including the given number of blocks (see column 3, line 25 to column 4, line 56).

Lee does not particularly disclose, though, a FIFO (First-In First-Out) memory arranged between the inverse quantizer and the zero-run reconstruction processor and configured to store the zero-run length data and nonzero coefficients, the memory operating with first-in first-out and having a memory capacity for storing coefficients contained in a plurality of blocks as claimed in claim 1. The particular use of memories for buffering of data so that the data could be timely processed, in general, is well recognized in the art. For example, Chida discloses an image communication apparatus as shown in Figure 3, and teaches the conventional use of FIFO memory 96 of Figure 3 for buffering data. Therefore, it would have been obvious to one of ordinary skill in the art, having the Lee and Chida references in front of him/her and the general knowledge of memory devices, would have had no difficulty in providing the FIFO memory 96 of Chida to be arranged between the inverse quantizer and zero run reconstruction processor of Lee so as to store the zero run length data and nonzero coefficients, the memory operating with first-in first-out and having a memory capacity for storing coefficients contained in a plurality of blocks for the same well known timely processing of decoded data purposes as claimed.

4. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Chida as applied to claims 1 and 2 in the above paragraph (3), and further in view of Kitayama (5,418,762).

The combination of Lee and Chida discloses substantially the same decoding apparatus as above, further including wherein the zero-run reconstruction device includes a buffer memory (i.e., 120 of Figure 1 of Lee) configured to write in the zero coefficients and nonzero coefficients, and wherein when the buffer memory writes in 58 to 62 percents of all coefficients corresponding to one block, the buffer memory reads out the coefficients (i.e., the reading and writing of data may be performed at any desired point, and as such the specifics as claimed do not add any patentable weight over reading/writing of data within buffer memory 120 of Figure 1 of Lee).

The combination of Lee and Chida does not particularly disclose, though, a buffer memory configured to write in the zero coefficients and nonzero coefficients therein at a write-in speed and read out them therefrom at a readout speed higher than the write-in speed as claimed in claim 3. The particular selective readout and writing speed of data within a memory, in general, is however old and well recognized in the art. For example, Kitayama teaches the particular readout of data from the memory higher than the speed at which data is written to the memory (see column 2, lines 19-63). Therefore, it would have been obvious to one of ordinary skill in the art, having the Lee, Chida, and Kitayama references in front of him/her and the general knowledge of read/write speeds of data within memory devices, would have had no difficulty in providing memory device involving the readout of data from the memory higher than the speed at which data is written to the memory as taught by Kitayama as part of the

memory characteristics within the buffer memory 120 of Figure 1 of Lee for the same well known control of reading and writing of data for timely processing purposes as claimed.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Chida as applied to claims 1 and 2 in the above paragraph (3), and further in view of Kohiyama et al (5,666,161).

The combination of Lee and Chida discloses substantially the same decoding apparatus as above, but does not particularly disclose wherein if nonzero coefficient does not exist at a final position of a block when the inverse quantizer receives a block end signal indicating the end of the block from the variable length decoder, the inverse quantizer generates a zero coefficient as the final DCT coefficient of the block as claimed in claim 4. The particular use of codes such as a zero coefficient and end of block signals in the case the nonzero coefficient does not exist at a final position of a block are however old and well recognized in the art, as exemplified by Kohiyama et al (see column 16, lines 28-46). Therefore, it would have been obvious to one of ordinary skill in the art, having the Lee, Chida, and Kohiyama references in front of him/her and the general knowledge of end of block signal generations within video encoders/decoders, would have had no difficulty in providing the codes such as a zero coefficient and end of block signals in the case the nonzero coefficient does not exist at a final position of a block all as part of the decoding processing within the inverse quantizer 116 of Lee for the same well known signaling of block completion processing purposes as claimed.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Chida as applied to claims 1 and 2 in the above paragraph (3), and further in view of Okada et al (5,854,799).

The combination of Lee and Chida discloses substantially the same decoding apparatus as above, but does not particularly disclose wherein the variable length decoder stops its output in units of one block when the inverse quantizer is unreceivable the zero-run length and nonzero coefficient from the variable length decoder as claimed in claim 5. However, such technical features are well known and made obvious by Okada et al (see Figure 2 and column 6, line 62 to column 7, line 19, column 7, line 60 to column 8, line 18, column 8, lines 37-45). Therefore, taking the combined teachings of Lee, Chida, and Okada et al, it would have been obvious to provide the stopping of the variable length decoder in the event the inverse quantizer is unreceivable of the zero run length and nonzero coefficient from the variable length decoder as taught by Okada et al as part of the video decoder of Lee for the same well known error detection and stopping of decoder functions so that the errors could be minimized and corrected purposes as claimed.

7. Claims 6, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Chida as applied to claims 1 and 2 in the above paragraph (3), and further in view of Okada et al (5,854,799).

The combination of Lee and Chida discloses substantially the same decoding apparatus as above, but does not particularly disclose wherein every time the inverse quantizer receives the zero run length from the variable length decoder, the inverse quantizer accumulates a value obtained by adding "1" to the zero-run length and generates scan address data indicating a

coefficient position of the nonzero coefficient, to generate quantization step size data every coefficient position based on the scan address data and scan pattern data indicating the scan pattern; wherein the inverse quantizer outputs to the first-in first-out memory DCT coefficient data indicating the inverse quantization result, the scan address data indicating a position of the DCT coefficient and the scan pattern data; and wherein the zero-run reconstruction processor includes an internal scan address counter increased one by one for each clock, and rejects next data input from the FIFO memory until a scan address received from the FIFO memory has coincided with a count value of the internal scan address counter, to generate the zero coefficients corresponding to the zero-run length as claimed in claims 6, 7, and 9. However, Jeong discloses a video decoder as shown in Figure 6, and teaches the conventional use of scan address data for indicating coefficient position of nonzero coefficients and scan pattern data indicating the scan pattern (see column 4, lines 43-55, column 6, lines 49-64). As such, it is considered obvious that the inverse quantizer 116 of Lee may accumulate any desired value, including adding "1" to the zero run length when receiving the zero run length data from the variable length decoder of Jeong to indicate the coefficient position of the nonzero coefficient. In addition, having provided the FIFO memory of Chida after inverse quantizer 116 of Lee, the inverse quantizer will output to the FIFO memory DCT coefficient data indicating the inverse quantization result, and the scan address data indicating a position of the DCT coefficient and the scan pattern data as provided by Jeong. Further, having provided the FIFO memory of Chida within Lee, it is considered obvious that the zero run reconstruction processor 118 of Lee must receive the proper scan address data before further processings. Therefore, some sort of counter, such as the internal scan address counter as claimed must be provided within the zero run

reconstruction processor of Lee to be increased one by one for each clock for timely processing, and wherein next data input from the FIFO memory is rejected until a scan address received from the FIFO memory has coincided with a count value of the internal scan address counter, to generate the zero coefficients corresponding to the zero run length, as claimed. Therefore, it would have been obvious to one of ordinary skill in the art, having the Lee, Chida, and Jeong references in front of him/her and the general knowledge of scan address data and scan pattern data generations for DCT coefficient data within video decoders, would have had no difficulty in providing the output from inverse quantizer 116 of Lee to the FIFO memory (i.e., as provided by Chida) DCT coefficient data indicating the inverse quantization result, the scan address data indicating a position of the DCT coefficient and scan pattern data, and an internal scan address counter within the zero run reconstruction processor 118 of Lee in view of the teachings of the scan addressing and scan pattern data processings of coefficients within the video decoder of Jeong for the same well known generation of quantization step size data for every coefficient position based on the scan address data and scan pattern data and timely processing of data between the zero run reconstruction processor 118 of Lee and FIFO memory (i.e., as provided by Chida before processor 118 of Lee) purposes as claimed.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Chida, and Jeong as applied to claims 1, 2, 6, 7, and 9 in the above paragraphs (3) and (7), and further in view of Okada et al (5,854,799).

The combination of Lee, Chida, and Jeong discloses substantially the same decoding apparatus as above, but does not particularly disclose wherein the inverse quantizer stops its output in units of one coefficient when the FIFO memory is unreceivable the data from the

inverse quantizer as claimed in claim 8. However, Okada et al teaches the conventional stopping of all decoding operations (i.e., 6-8 of Figure 2, see column 3, lines 33-56, column 6, line 62 to column 7, line 19, column 7, line 60 to column 8, line 45) in the event that error(s) have arose in the variable length decoding or dequantization processes. Though Okada et al does not particularly teach that the inverse quantizer will stop its output in units of one coefficient when the FIFO memory is unreceivable the data from the inverse quantizer, it is however considered obvious that if the FIFO memory of Chida as provided within the Lee is unreceivable of the inverse quantized data, this will trigger the inverse quantizer to stop its operation in view of Okada et al's teaching that all decoding operations will stop if an error is found in one of the decoding components. Therefore, it would have been obvious to one of ordinary skill in the art, having the Lee, Chida, Jeong, and Okada et al references in front of him/her and the general knowledge of video decoder error and stopping of operations based on the error, would have had no difficulty in stopping the inverse quantizer of Lee in units of one coefficient when the FIFO memory (i.e., as provided by Chida) is unreceivable the data from the inverse quantization in view of the teachings of Okada et al involving the stopping of all decoding operations in the event of an error in the video decoding process.

9. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 12-19 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

11. The following is an Examiner's Statement of Reasons for Allowance:

Claims 12-19 are considered allowable over the prior art of record because the prior art of record does not particularly suggest, disclose, or teach a decoding apparatus configured to decode compression-encoded video data including a variable length code, comprising a plurality of decompression devices configured to decompress compression-encoded video data corresponding to a plurality of channels, respectively, each of the decompression devices including particularly a zero run reconstruction processor, a FIFO memory, a plurality of parameter extractors provided corresponding to the decompression devices, and configured to generate parameters concerning one macroblock ever time the variable length decoder included in each of the decompression devices completes decoding of one block, and a motion compensator which subjects the transformed coefficients to a motion compensation in accordance with the parameters concerning one block input from the parameter extractors alternately as claimed in claim 12.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jeon et al, Kim et al, Suzuki, Obayashi et al, Kim, and Tanaka et al, and Shimoda disclose various types of video coders and decoders.

13. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry)

(for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Lee whose telephone number is (703) 308-6612. The Examiner can normally be reached on Monday to Friday from 8:00 a.m. to 5:30 p.m, with alternate Fridays off.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group customer service whose telephone number is (703) 306-0377.

RICHARD LEE
PRIMARY EXAMINER

Richard Lee/rl

3/5/04